Z8581 Clock Generator and Controller

October 1988

FEATURES

- Two independent 20 MHz oscillators generate two 10 MHz clock outputs and one 20 MHz clock output.
- Oscillator input frequency sources can be either crystals or external oscillators.
- Outputs directly drive the Z80, Z8000, 8086, 8088, and 68000 microprocessor clock inputs.
- Can be used as a general-purpose clock generator.
- 18-pin slimline package used; single +5V dc power required.
- Provides ability to stretch High and/or Low phase of clock signal under external control.
  - On-chip 2-bit counter can be used to selectively stretch clock cycles.
- On-chip reset logic
  - Reset output is synchronized with System Clock output.
  - Power-up reset period is maintained for a minimum of 30 ms.
  - External input initiates system reset.

GENERAL DESCRIPTION

The Z8581 Clock Generator and Controller is a versatile addition to Zilog's family of Universal microprocessor components. The selective clock-stretching capabilities and variety of timing outputs produced by this device allow it to easily meet the timing design requirements of systems with microprocessors and LSI peripherals. The clock output drivers of the Z8581 also meet the non-TTL voltage requirements for driving NMOS clock inputs with no additional external components. The Z8581 provides an elegant, single-chip solution to the design of system clocks for microprocessor-based products.

The Z8581 oscillators are referenced as the system clock oscillator and the general-purpose clock oscillator. Both oscillators are driven by external crystals or other frequency sources.

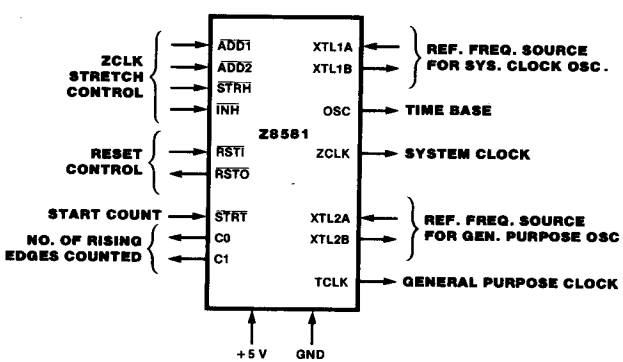


Figure1. Pin Functions

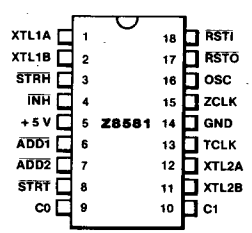


Figure 2. Pin Assignments

PIN DESCRIPTIONS

Figures 1 and 2, respectively, show the pin functions and assignments of the Z8581. Tie unused inputs High through a resistor.

$\overline{\text{ADD1}}$, $\overline{\text{ADD2}}$. *Add Delay 1* (input, active Low) and *Add Delay 2* (input, active Low). These signals control the addition of one, two, or three delay periods to a selected half-cycle of the ZCLK output.

C0, C1. *ZCLK Count 0* (output, active High) and *ZCLK Count 1* (output, active High). These signals indicate, in binary, the number or rising edges of ZCLK that have occurred after the assertion of the $\overline{\text{STRT}}$ input.

$\overline{\text{INH}}$. *Inhibit Delay* (input, active Low). When asserted, this signal inhibits the functions of inputs $\overline{\text{ADD1}}$ and $\overline{\text{ADD2}}$.

OSC. *Time Base Clock* (output, active High). This signal provides a TTL-compatible clock output at the same frequency as the system clock frequency source.

$\overline{\text{RSTI}}$. *Reset In* (input, active Low). When asserted, this signal indicates a reset condition and initiates the assertion of $\overline{\text{RSTO}}$ synchronized with ZCLK.

$\overline{\text{RSTO}}$. *Reset Out* (output, active Low). When asserted, this signal indicates that a system reset condition is required, either by $\overline{\text{RSTI}}$ going Low or by a system powerup condition.

$\overline{\text{STRT}}$. *Start Count* (input, negative edge-triggered). When asserted, this signal resets a two-bit binary counter and then enables the counter to count the rising edges of the ZCLK output.

$\overline{\text{STRH}}$. *Delay ZCLK* (input, active Low). When asserted, this signal causes the current half-cycle of the ZCLK output to be delayed (stretched) for as long as $\overline{\text{STRH}}$ is held Low. This control input overrides the $\overline{\text{ADD1}}$, $\overline{\text{ADD2}}$, and $\overline{\text{INH}}$ functions.

TCLK. *General-Purpose Clock* (output, MOS-compatible, active High). This signal is the timing output of the general-purpose oscillator. TCLK's frequency is half that of the external oscillator used to drive the general purpose oscillator.

XTAL1A, XTAL1B. *System Clock Frequency Source A* (input, active High) and System Clock Frequency Source B (output, active High). These signals are used by the external oscillator to drive the internal system clock oscillator and the OSC output.

XTAL2A, XTAL2B. *General-Purpose Clock Frequency Source A* (input, active High) and *General-Purpose Clock Frequency Source B* (output, active High). These signals are used by the external oscillator to drive the internal general-purpose clock oscillator.

ZCLK. *System Clock* (output, MOS-compatible, active High). This signal is the timing output of the system clock oscillator. This clock can be modified by the delay (stretch) control inputs. Its frequency, when unmodified, is half that of the external system clock frequency source.

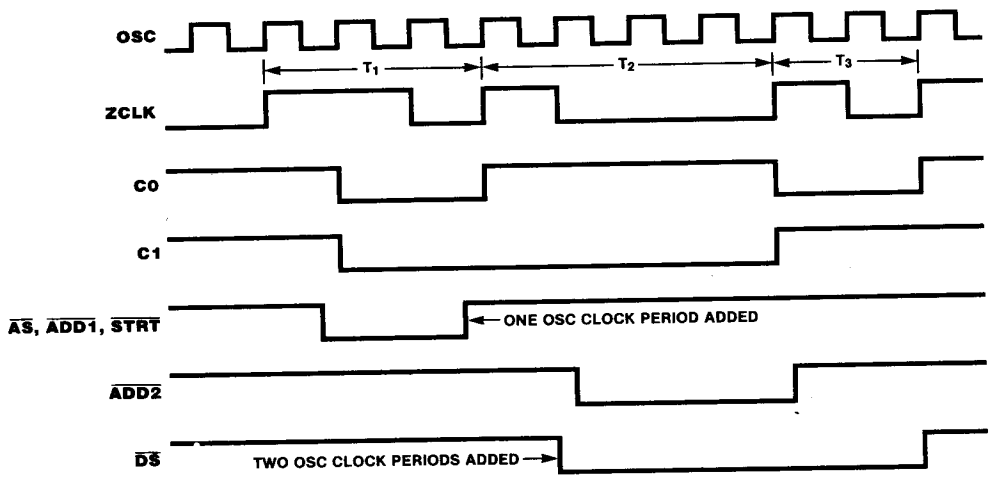


Figure 3. Timing Diagram Stretching Z8000 AS and DS

System Clock Oscillator

The timing outputs provided by this oscillator consist of a Time Base output (OSC), at the frequency of the reference source, and a stretchable System Clock output (ZCLK), at a frequency determined by the stretch control inputs. An on-chip TTL driver at OSC and an NMOS driver at ZCLK eliminate the need for external buffers or drivers. The NMOS drivers can drive 200 pf loads with output rise and fall times of 10 ns maximum.

ZCLK can be stretched under program or hardwired control by selectively adding periods equivalent to a full OSC cycle to either the High or Low portion of a clock cycle. One, two, or three periods can be added to double, triple, or quadruple the duration of the selected ZCLK half-cycle. Adding periods to ZCLK is a function of the ADD1 and ADD2 inputs. These active Low inputs are sampled prior to the rising edge of signal OSC; their sampled status represents the number of periods to be added to ZCLK.

Two additional control inputs, $\overline{INH}$ and $\overline{STRH}$, affect the stretch function. Input $\overline{INH}$, when asserted, inhibits the function of $\overline{ADD1}$ and $\overline{ADD2}$. Input $\overline{STRH}$ stretches the ZCLK output for as long as it is asserted (Low); it overrides all other stretch control inputs.

Table 1 summarizes the functions performed by the stretch control inputs.

The system clock oscillator also contains a 2-bit ZCLK counter. This counter, when initialized by the assertion of $\overline{STRT}$, counts the next four rising edges of the ZCLK output. The current count is presented on outputs C0 and C1. This counter and its outputs enable the user to determine the occurrence (rising edge) of each of four clocks after a specific event ($\overline{STRT}$ is asserted). This facility can, for example, be used to determine when a delay is to be inserted into a CPU machine cycle when $\overline{STRT}$ is triggered by either an $\overline{M1}$ (Z80) or an $\overline{AS}$ (Z8000) input signal.

The clock stretch capability allows systems to run at the nominal high speed of ZCLK, except during cycles that require more time than usual to complete a transaction. For example, extended access time may be required in accessing certain areas of memory, in accessing I/O devices, or in other CPU/Peripheral transactions. Figures 3 and 4 illustrate, respectively, the circuit configuration and timing required to stretch the Z8000 Address Strobe ($\overline{AS}$) and Data Strobe ($\overline{DS}$) to allow more time for address functions and to enable the CPU to operate with memories that have a relatively long access time.

In addition, the ZCLK stretch control logic can be hardwired to meet various duty cycle requirements. For example, a simple hardwired connection can cause every other ZCLK cycle to be stretched to produce a ZCLK output with a 33% duty cycle.

The system clock oscillator also provides a system reset output ($\overline{RSTO}$) that is synchronized with ZCLK. This output is controlled by a system reset input ($\overline{RSTI}$) during normal system reset operations and by delay circuitry in the system clock oscillator during power-up operations. During a normal system reset operation, a Low on $\overline{RSTI}$ causes $\overline{RSTO}$ to be asserted (Low) on the next rising edge of ZCLK. Output $\overline{RSTO}$ is held Low for a period of 16 ZCLK clock cycles (the required reset time for both the Z80 and Z8000 CPU system reset functions). During a power-up operation, $\overline{RSTO}$ is asserted for a minimum of 30 ms after power is turned on (the time required for both the Z80 and Z8000 power-up functions).

Table 1. Stretch Control Functions

STRH	INH	ADD2	ADD1	Periods Added
0	X	X	X	Unlimited
1	0	X	X	0
1	1	0	0	3
1	1	0	1	2
1	1	1	0	1
1	1	1	1	0

NOTES: X = Don't Care, 1 = High, 0 = Low

General-Purpose Oscillator

This oscillator provides a fixed frequency General-Purpose Clock output (TCLK) at half its source frequency. This output is useful for system timing functions such as controlling a baud rate generator. Output TCLK can also be used as the frequency reference source for the system clock oscillator.

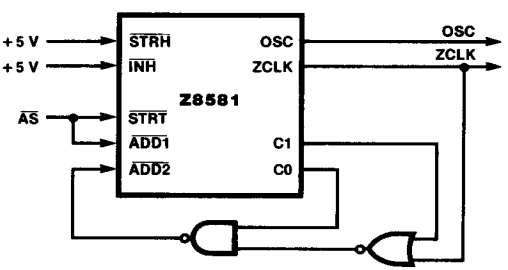


Figure 4. Configuration for Stretching Z8000 Address (AS) and Data (DS) Strobes

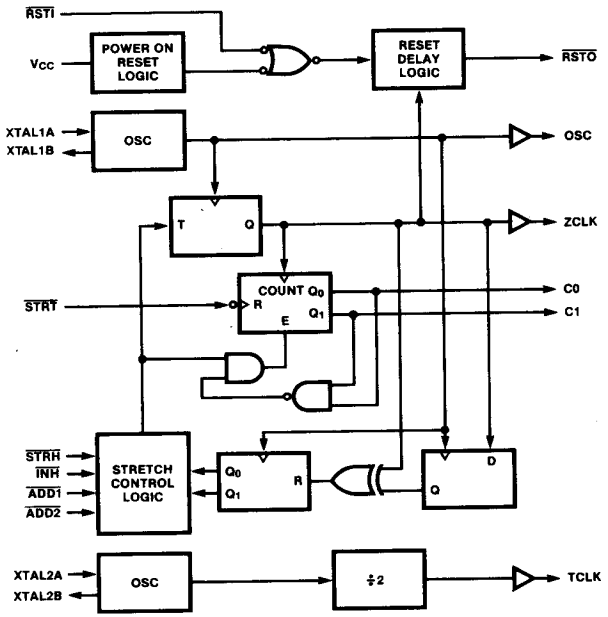
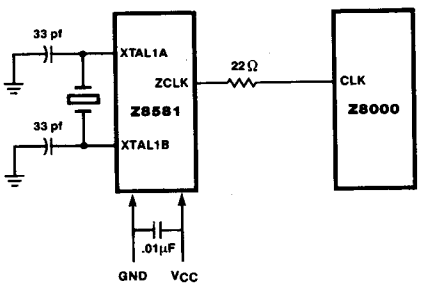


Figure 5. Z8581 Functional Block Diagram

SYSTEM INTERFACE CONSIDERATIONS

Due to the fast rise and fall times produced by the Z8581, transmission line concepts must be applied in order to avoid ringing and reflections on the clock outputs. More specifically, the interconnections between the clock outputs and the loads they are driving must be treated as transmission lines, and it is necessary to match the source impedance of the clock outputs to the characteristic impedances of these transmission lines. In most cases the impedances can be matched by placing termination resistors in series with the clock outputs. These resistors range in value from 22 to 220 ohms, with the value chosen to optimize the clock risetime at the load. **(See Figure 6.)** It is important to control the impedance seen by the clock output by keeping leads short and avoiding stray inductances wherever possible.

Another important consideration is the bypass capacitor. To avoid distortion of the power supply, the Z8581 requires a high frequency 0.01 μF ceramic capacitor between V_{CC} and ground, and the leads connecting this capacitor to the pins should be kept as short as possible.



NOTE: The Z8581 requires a parallel-resonant fundamental type crystal. The capacitor may be varied to fine tune the frequency.

Figure 6. Z8581/Z8000 Interface

SERIES RESONANCE AND PARALLEL RESONANCE

Manufacturers of crystals specify crystals as either series-resonant or parallel-resonant **(Figure 7.)**.

At the frequency of series resonance:

$$fs = \frac{1}{2\pi\sqrt{L*C}}$$

When the magnitude of X_C (reactance of C) and X_L (reactance of L) are equal, one effectively cancels the other, resulting in an equivalent of R shunted by Cs. If R is very small compared to X_{Cs}, series resonance is indicated by minimum impedance and zero phase shift. The series-resonant crystals are resistive and produce an output in phase with the input.

At frequencies slightly higher than series resonance, X_L increases and X_C decreases, resulting in a net inductive reactance, X_L. When $X_L = X_{Cs}$, the result is parallel resonance with the frequency of parallel resonance:

$$fp = \frac{1}{2\pi\sqrt{L*\frac{C*C_s}{C+C_s}}}$$

Parallel resonance is indicated by maximum impedance across the crystal terminals. Parallel-resonant crystals are inductive and produce the output shifted in phase from the input.

If a series crystal is used with a parallel-resonant oscillator, the crystal is forced to operate in the parallel region (and vice versa). The clock frequency produced is shifted a small percentage (about 350 ppm) from the specified series crystal frequency **(Figure 7.)**. Any attempts to fine tune the frequency by changing the value of external capacitance may cause the crystal to stop oscillating.

From the equivalent circuit of the crystal and the expression of fs, it can be seen that the series-resonant frequency of the crystal cannot be changed by reactance across the crystal terminals because there is no connection to the junction of L and C. In the case of parallel resonant frequency, Cs appears in the expression and its effective value can be changed by reactance across the terminals.

The load capacitance (C_L) is the capacitance that the crystal sees at its terminals. In parallel-resonant mode, load capacitance is very important, because C_L in combination with crystal inductance determines the frequency.

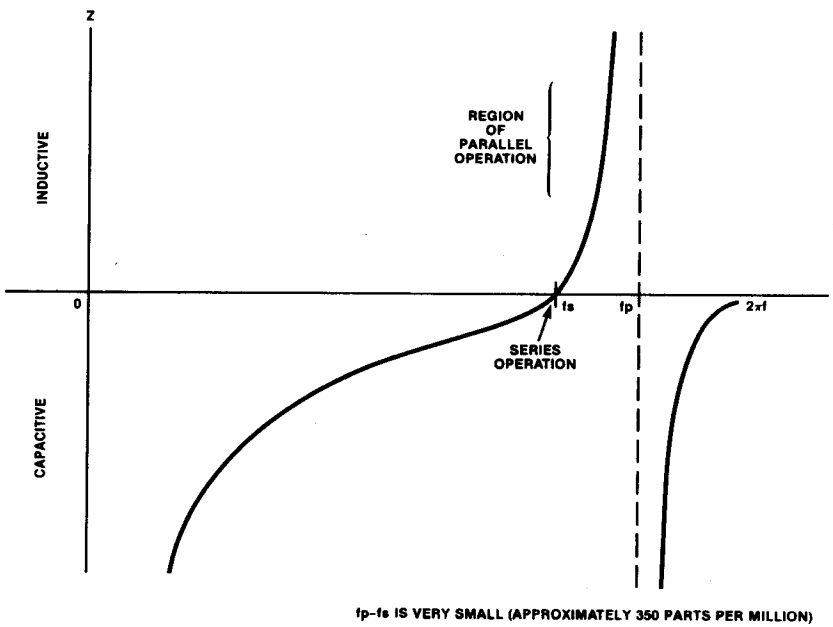


Figure 7. Series vs. Parallel Resonance

Crystal selection is based on the oscillator design used to provide the clock to the system. Series-resonant crystals should be used with non-inverting oscillators because series-resonant crystals have no phase shift. Parallel-resonant crystals should be used with inverting oscillators because parallel-resonant crystals have some phase shift due to their inductive nature.

DRIVE LEVEL

Drive level is critical because the crystal can dissipate only limited power (10 mW typical) and still meet all specifications. Overdrive may cause the temperature to rise in the crystal. Further overdrive may cause the quartz to operate in a non-linear region producing a frequency shift and possibly causing permanent damage to the crystal.

SERIES CONFIGURATION

When the internal oscillator is non-inverting, the recommended crystal is series-resonant and the circuit **diagram shown in Figure 8. is used**

Many supposedly series-resonant IC oscillators actually operate below series resonance. C1 is used to compensate for this inductive nature of the series-type oscillator. C1 provides enough capacitive reactance to cancel the inductive shift caused by the IC. This brings the overall frequency back to series resonance.

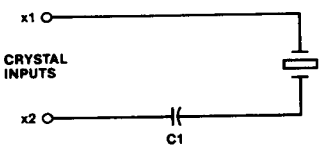


Figure 8. Circuit for Series-Resonant Crystals

PARALLEL CONFIGURATION

When the internal oscillator is inverting, the recommended crystal is parallel-resonant and the circuit diagram **shown in Figure 9. is used.**

The load capacitance, C_L, is determined by the following equation:

$$C_L = \frac{C_1 * C_2}{C_1 + C_2} + C_C$$

where C_C is the parasitic circuit capacitance.

The parallel resonance frequency is determined by the following equation:

$$fp = \frac{1}{2\pi \sqrt{L^* \frac{C * C_t}{C + C_t}}}$$

where $C_t = C_L + C_S$

Typically, the value of C_L ranges between 20pf and 30pf, and the value of the ratio C1/C2 ranges between 1 and 2. The required frequency can be fine tuned by varying the value of C2. The value of C_L, derived from C1 and C2, depends on the required frequency, characteristics of the oscillator, and the crystal used.

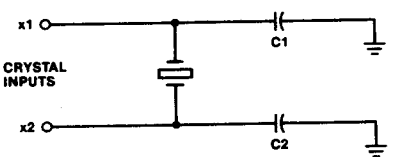


Figure 9. Circuit for Parallel Resonant Crystals

RECOMMENDED CIRCUIT FOR Z8581

Since the internal oscillator of the Zilog Z8581 is inverting, a parallel-resonant type crystal is recommended. The circuit configuration is shown in figure 10. The preferred value of the C_L is about 22pf. The preferred value of C1 and C2 is 33pf, which produces a ratio (C1/C2) of one. C2 can be made variable to fine tune the required frequency.

The output of one oscillator can also be connected to the crystal inputs of the second oscillator, using a 4700 ohms pull-up resistor at the output. (Figure 10.).

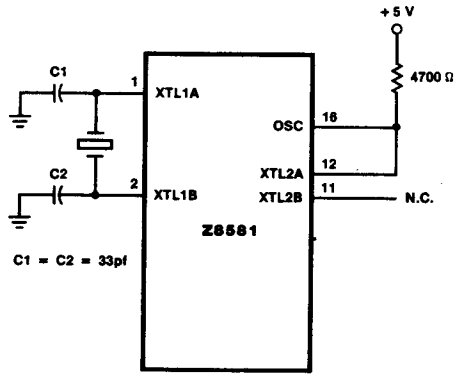


Figure 10. Circuit Configuration for Z8581

SPECIFICATIONS

For proper operation when using Zilog's Z8581, use a fundamental, parallel-type crystal. The following crystal specifications are suggested:

Frequency tolerance: Application dependent
C_L, load capacitance: Approximately 22pf (acceptable range is from 20-30pf)
Rs, equivalent-series resistance: © 150 ohms
Drive level
(for © 10 MHz crystal): 10 milliwatts
(for □ 10 MHz crystal): 5 milliwatts

Holder specifications are user-determined.

For frequencies lower than 4 MHz, the recommended holder type is HC-33/U (0.75"W × 0.765"H, 1.5" lead length with specing of 0.486").

For frequencies higher than 4 MHz, the recommended holder type is HC-18/U (0.435"W × 0.530"H, 1.5" lead length with specing of 0.192").

SUGGESTED VENDORS

The wide variety of applications and frequencies in which crystals are used makes it necessary to custom manufacture all but a very few crystal types. With the crystal specifications given above, most vendors can make the desired crystal even though it may not be a standard off-the-shelf item.

The following two vendors supply crystals to the specifications given above. The user is not limited to these vendors because these suppliers are among many suppliers who might meet your specifications.

Midland-Ross Corporation
NEL UNIT
357 Beloit Street
Burlington, WI 53105
Telephone: (414) 763-3591

CTS KNIGHTS, INC.
400 E. Reimann Ave.
Sandwich, Illinois 60548
Telephone: (815) 786-8411

ABSOLUTE MAXIMUM RATINGS

Voltages on all inputs and outputs with respect to GND . . . . . −0.3V to +7.0V
Operating Ambient Temperature. . . . . See ordering information
Storage Temperature . . . . . −65°C to +150°C

Stresses greater than those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only: operation of the device at any condition above those indicated in the operational sections of these specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

The Ordering Information section lists package temperature ranges and product numbers. Refer to the Literature List for additional documentation. Package drawings are in the Package Information section.

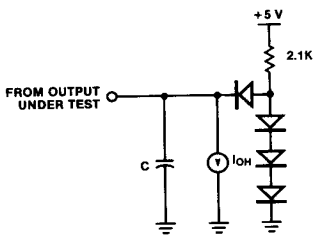
STANDARD TEST CONDITIONS

The DC characteristics below apply for the following standard test conditions, unless otherwise noted. All voltages are referenced to GND (0V). Positive current flows into the referenced pin.

Available operating temperature ranges are:

- S = 0°C to +70°C, $+4.75V \leqslant V_{CC} \leqslant +5.25V$
- E = −40°C to +85°C, $+4.5V \leqslant V_{CC} \leqslant +5.25V$
- M = −55°C to +125°C, $+4.5V \leqslant V_{CC} \leqslant +5.5V$

All ac parameters assume a total load capacitance (C), including parasitic capacitances, of 100 pf max, except for parameters 8, 9, 21, and 22 which are 200 pf max. Timing references between two output signals assume a load difference of 50 pf max.



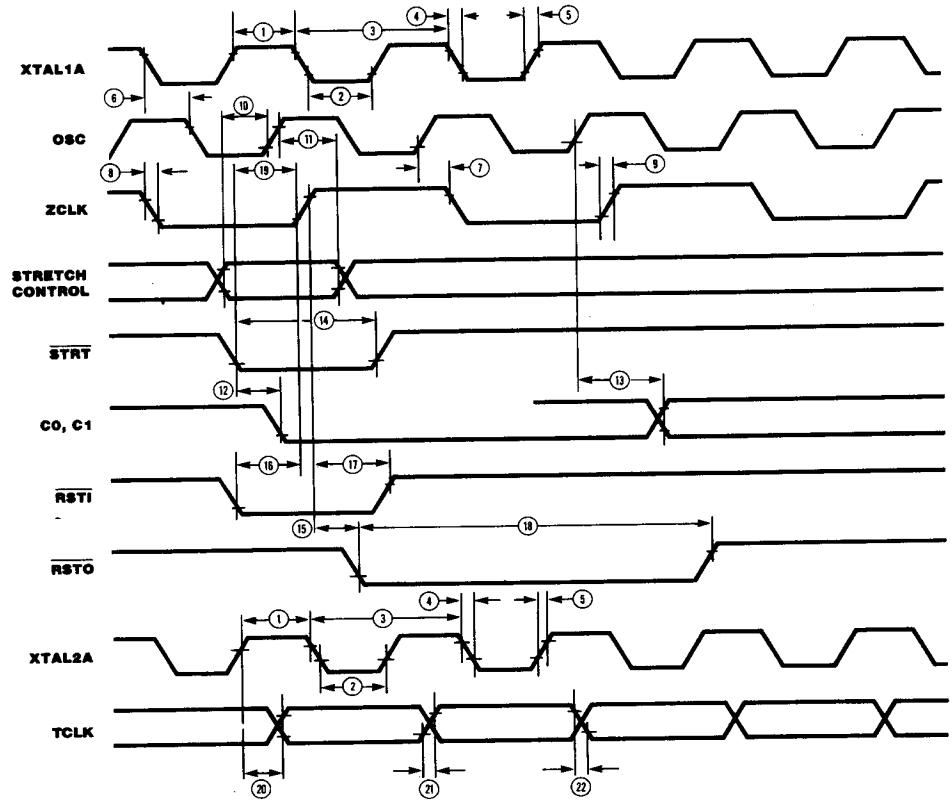
DC CHARACTERISTICS

Symbol	Parameter	Min	Max	Unit	Condition
V_{CH}	Clock Input High Voltage	V_{CC} −3.7	V_{CC} + 0.3	V	Driven by External Clock Generator
V_{CL}	Clock Input Low Voltage	−0.3	0.45	V	Driven by External Clock Generator
V_{IH}	Input High Voltage	2.0	V_{CC} + 0.3	V	
V_{IL}	Input Low Voltage	−0.3	0.8	V	
V_{OH}	Output High Voltage	2.4		V	I_{OH} = −250 μA
V_{OH} (ZCLK, TCLK)	Output High Voltage	V_{CC} − 0.3		V	I_{OH} = −250 μA tested at 5 μs after ZCLK or TCLK rises High
		2.4		V	I_{OH} = −250 μA
V_{OL}	Output Low Voltage		0.4	V	I_{OL} = = +2.0 mA
I_{IL}	Input Leakage		±10	μA	$0.4 \leqslant V_{IN} \leqslant +2.4V$
I_{CC}	V_{CC} Supply Current		150	mA	

AC CHARACTERISTICS

Number	Symbol	Parameter	Z8581 6 MHz Min.	Z8581 6 MHz Max.	Z8581-10 10 MHz Min	Z8581-10 10 MHz Max	Units	Notes[1]
1	TwCH	Clock Input High Width	31		18		ns	2
2	TwCL	Clock Input Low Width	31		18		ns	2
3	TpC	Clock Input Cycle Time	82		50		ns	2
4	TfC	Clock Input Fall Time		10		7	ns	2
5	TrC	Clock Input Rise Time		10		7	ns	2
6	TdOSC	Clock Input to OSC Delay		30		20	ns	
7	TdZC	OSC to ZCLK Delay		20		15	ns	
8	TfZC	ZCLK Fall Time		10		10	ns	
9	TrZC	ZCLK Rise Time		10		10	ns	
10	TsSC	Stretch Controls to OSC ↑ Setup	35		20		ns	
11	ThSC	Stretch Controls to OSC ↑ Hold	20		20		ns	
12	Td(ST/CR)	STRT ↓ to 2-bit Counter Reset Delay		35		25	ns	
13	Td(OSC/CC)	OSC ↑ to 2-bit Counter-Change		20		17	ns	3
14	Tw(STRT)	STRT Low Width	50		30		ns	
15	Td(RSTO)	ZCLK ↑ to RSTO ↓ Delay		30		20	ns	
16	Ts(RSTI)	RSTI ↓ to ZCLK ↑ Setup	30		20		ns	
17	Th(RSTI)	RSTI ↓ to ZCLK ↑ Hold	30		20		ns	
18	Tw(RSTO)	RSTO Low Width	16		16		cycles	
19	Ts(ST/ZC)	STRT ↓ to ZCLK ↑ Setup to include ZCLK edge	40		30		ns	
20	TdTC	Clock Input to TCLK Delay		40		30	ns	
21	TrTC	TCLK Rise Time		10		10	ns	
22	TfTC	TCLK Fall Time		10		10	ns	

NOTES: 1. All timings are preliminary and subject to change.
2. Clock input other than a crystal oscillator.
3. Assuming ZCLK rising.



Timing measurements are made at the following voltages:

	High	Low
ZCLK, TCLK	4.0V	0.8V
Output	2.0V	0.8V
Input	2.0V	0.8V