Order this document
by MC68450AD/D

MOTOROLA
SEMICONDUCTOR
TECHNICAL DATA

Addendum to

MC68450
Direct Memory Access Controller

The following information applies to ADI1216, *MC68450 Direct Memory Access Controller (DMAC)* Advance Information Data Sheet for the ***A84G Mask only***:

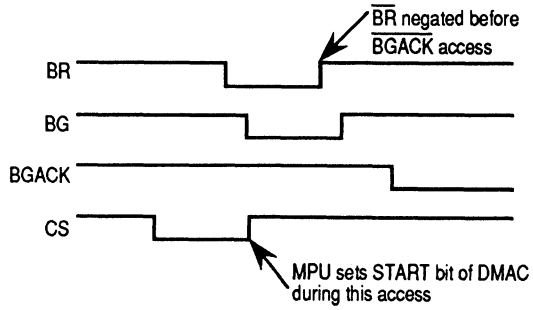
1. When not using the function code lines, these lines must be kept high by using pullup resistors.

2. When the following two conditions occur simultaneously, incorrect data is supplied by the DMAC during the write cycle immediately following the negation of the relinquish and retry (R&R) exception:
   a. R&R is asserted at the write cycle in the dual address mode.
   b. MPU access to the DMAC's internal register is performed after the DMAC relinquishes the bus due to the R&R exception.

   Suggested countermeasures are as follows:
   a. Assert R&R exception only during the read cycle when using dual addressing mode.
   b. If the R&R exception occurs during the write cycle of the dual addressing mode, avoid accesses to the DMAC's registers.
   c. Use the HALT exception instead of R&R exception to access the DMAC's internal registers.

3. If the MPU asserts $\overline{CS}$ of the DMAC when the DMAC has its $\overline{BR}$ asserted, then the DMAC negates its $\overline{BR}$. (This timing does not cause any problems when used directly with an M68000 MPU. This is a consideration for designs external bus arbiters.)

4. When the MPU sets the START bit of the DMAC and a different channel is already active in the limited rate auto-request mode (LRAR), then the following bus arbitration timing may occur:

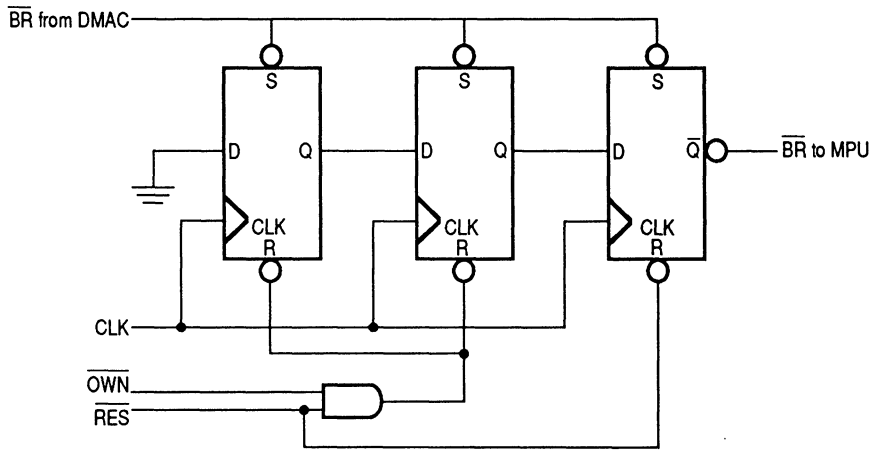


This timing diagram shows that the $\overline{BR}$ is negated too early and may cause a bus contention between the MPU and DMAC. The problem occurs in the following conditions:

a. Two or more channel are in operation.
b. One of the channels is in the LRAR.
c. The priority level of the LRAR channel is higher than or equal to the other channels.
d. The LRAR channel is initiated before the other channels.

Suggested countermeasures are as follows:

a. Set the priority of the LRAR channel to the lowest level. If two or more channels are set to LRAR, a lower priority channel should be initiated first.
b. External latches should be provided for as shown in the following diagram:



5. No DMAC register must be accessed sooner than seven DMAC clock cycles after setting the STR bit of the CCR.

6. When $\overline{\text{HALT}}$ ($\overline{\text{BEC}}$ input) is asserted to halt an active channel operation and then the STR bit is set to start another channel, neither channel asserts the $\overline{\text{BR}}$, and the entire DMAC operation stops. However, these modes operate correctly under the following constraints:
   a. Single addressing mode, except when $\overline{\text{HALT}}$ ($\overline{\text{BEC}}$ input) is asserted during the last bus cycle of any channel.
   b. Dual addressing mode, 16-bit operand size, 16-bit port size, except when $\overline{\text{HALT}}$ ($\overline{\text{BEC}}$ input) is asserted during the last bus cycle of any channel.

   Suggested countermeasures are as follows:
   a. When new channels are started by setting the STR bit by asserting $\overline{\text{HALT}}$, these conditions should be met:
      Assert the $\overline{\text{REQ}}$ input to the channel that was halted.
      Set the priority level of the newly started channel lower than the halted channel.
   b. The following procedure is suggested when setting the STR bit of other channels by halting the DMAC:
      Assert $\overline{\text{HALT}}$ ($\overline{\text{BEC}}$ input).
      Set the $\overline{\text{HLT}}$ bit of the CCR of all active channels.
      Negate $\overline{\text{HALT}}$ ($\overline{\text{BEC}}$ input).
      Set the STR bit to start the new channel.
      Reset the $\overline{\text{HLT}}$ of the other channels.
   c. Use single addressing mode whenever possible and do not set the STR bit of other channels when the $\overline{\text{HALT}}$ is performed during the last DMA bus cycle of a channel.

7. An incorrect vector may be returned under these conditions:
   a. One channel asserts $\overline{\text{IRQ}}$.
   b. A different channel is being serviced with an active bus cycle.
   c. The MPU runs an $\overline{\text{IACK}}$ cycle (in parallel with the DMA cycle) and causes $\overline{\text{HALT}}$ ($\overline{\text{BEC}}$ input) to be asserted to the DMAC.

   The vector returned is that of the channel running the bus cycles rather than the channel actually requesting the interrupt.

8. When using LRAR, the GCR must be set so that the LRAR burst time is at least (12.5 clocks) + (one MPU read cycle). LRAR burst time refers to the length of time the internal auto-request signal is asserted.

9. When using LRAR, assert the $\overline{\text{BEC}}$ lines for bus exceptions only when the DMAC has the bus ownership (i.e., $\overline{\text{BGACK}}$ bit of DMAC is asserted).

10. An operation timing error might occur on an attempt to program the SCR and CCR using a single 16-bit bus cycle instead of two, separate, 8-bit bus cycles.

Literature Distribution Centers:

USA: Motorola Literature Distribution; P.O. Box 20912; Phoenix, Arizona 85036.
EUROPE: Motorola Ltd.; European Literature Center; 88 Tanners Drive, Blakelands, Milton Keynes, MK14 5BP, England.
ASIA PACIFIC: Motorola Semiconductors H.K. Ltd.; P.O. Box 80300; Cheung Sha Wan Post Office; Kowloon Hong Kong.
JAPAN: Nippon Motorola Ltd.; 3-20-1 Minamiazabu, Minato-ku, Tokyo 106 Japan.

A18666-2 PRINTED IN USA 7/89 IMPERIAL LITHO C66104 12.000 MPU