

An NS32CG160-Based Circuit with Static RAM

National Semiconductor
Application Note 733
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September 1990



An NS32CG160-Based Circuit with Static RAM

1.0 INTRODUCTION

This application note shows a basic configuration of a circuit based on the NS32CG160 processor. This circuit includes the NS32CG160, Static RAM and EPROM, data buffers, address latches and control.

This circuit is designed to work at 25 MHz with no wait states for 55 ns access time SRAM, and with three wait states for 200 ns access time EPROM. This document will also present the number of wait states needed for other speeds of memory.

2.0 SYSTEM DESCRIPTION

2.1 General Description

The major parts of the system are:

- The CPU circuit—including the NS32CG160-25, the reset circuit and an oscillator.
- The address latch/buffer—including two 74AS373 units, and one 74AS244 unit.
- The data buffers—including two 74F245 units.
- The memory control—including PAL 20R6__10, PAL 16R4__10, 74AS74.
- The SRAM part—including four P4C188__55 units.
- The EPROM part—including two NMC27C512-20 units.

2.2 CPU Circuit

- Power and Grounding—connecting all V_{CC} pins to +5V, and all GND pins to ground.
- Oscillator—a XTAL, whose frequency is twice the CPU clock frequency, should be connected to OSCIN.
- Reset circuit—a simple RC circuit whose time base is more than 50 μ s.
- Pull up resistor on unused inputs—pull up resistor needed on \sim NMI, \sim CWAIT, \sim HOLD, \sim IR0: \sim IR3, \sim DRQ0: \sim DRQ1, \sim EOT.

2.3 Address Latch

The two 74AS373 units create a 16 bits transparent latch with TRI-STATE outputs. They latch A0:A15 from AD0:AD15 during T1, and keep them stable until the end of the transaction. The Latch-enable input is connected to ALE.

The lines A16:A23 are buffered on the way to the other system elements.

2.4 Data Buffers

The two 74F245 units create a 16 bits bidirectional transceiver with TRI-STATE outputs. These bidirectional transceivers are used to buffer D0:D15 between CPU and memory. The direction is controlled by \sim DDIN, and the Output-enable input is connected to \sim DBE.

2.5 Memory Control

When we want to organize the memory map we should consider two opposite demands. The first demand is that we have a ROM at address 0, because after reset the CPU goes to address 0 in order to fetch instructions. The second demand is that we have a RAM at the low 64 kbytes of memory, because the MOD register is 16 bits length. In order to handle these two demands we use a SHADOW mechanism. The RAM is mapped at address 0x0 and the ROM is mapped at address 0x800000. At reset, a flag called \sim SHAD is set (low). When this flag is low every access to the low part of memory will be from the ROM. The first instructions of the user program on the ROM should be a jump command to the real ROM address and then reset the \sim SHAD flag (high). The flag is reset when writing to a dedicated address in the memory space so \sim CSSH (Chip Select SHadow) has low to high transaction, this line is used as clock pulse to 74AS74 (D flip-flop) whose D input is high.

Example:

The RAM addresses are 0x000000-0x007FFF
The ROM addresses are 0x800000-0x81FFFF
The shadow hardware addresses are 0xF60000-0xF7FFFF
 \sim SHAD = 0 (system after reset)

The assembly code is:

```
jump@(begin + 0x800000)
    "this line changes the PC to the real ROM address
begin:movb $0, @0xF70000 "this line reset  $\sim$ SHAD (high)
The 20R6__10 (ADEC) is a PAL that generates Chip Select signals.
```

The 16R4__10 (WAIT) is a PAL that controls Wait states generation.

The Chip-Select signals are based on address lines (A17:A23, A0, \sim HBE) and control lines (\sim TSO, \sim ADSS, \sim SHAD, \sim DDIN). We use \sim ADSS (\sim ADS used as clear input to D flip-flop whose D input is high) and \sim TSO to generate a pulse identify the R.E. of T2. We use a state machine in order to give Enable at R.E. of T2 when the address is stable, and to have maximum access time to memory. The Wait lines gives a constant number of wait states depending on the kind of memory we use. The PALs may be changed if the wait states number increases. For more details see: 3. PAL EQUATION.

2.6 SRAM

In this system we use four units of 16K x 4-bit SRAM which create a 16 bits data bus divided into two groups. The first group includes D0:D7, the second group includes D8:D15.

The addresses of SRAM are 0x000000:0x007FFF.

The address space of these units is 16K words, therefore every unit gets A1:A14 as address lines.

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The difference in Chip Selects between the two groups is that the first group (low DATA BUS) is active when A0 is low, and the second group (high DATA BUS) is active when \sim HBE is low. In that way we can access a byte or a word. The number of wait states needed in read or write cycles depends on the SRAM access time. The following table summarizes some of the options.

Speed	Read Cycle	Write Cycle	Notes
55 ns or Less	0 Wait States	0 Wait States	Used in This System
70 ns	1 Wait States	0 Wait States	—

2.7 EPROM

In this system we use two units of 64K x 8-bit EPROM which create a 16-bit data bus. We always read all 16 bits together.

The address space of these units is 64K word, therefore every unit gets A1:A16 as address lines.

The addresses of the EPROM are 0x800000:0x81FFFF.

The number of wait states needed in read cycle depends on the EPROM access time. The following table summarizes some of the options.

Speed	Read Cycle	Notes
200 ns	3 Wait States	Used in This System
170 ns	3 Wait States	—
150 ns	2 Wait States	—

3.0 PAL EQUATION

```
module adec
flag '-r3' , '-t2' , '-s' , '-q2'

title 'APPLICATION NOTE : CPU:=NS32CG160 , MEMORY:=SRAM,EPROM '

" Author : Yiftach Shinar
" Date   : 13 May 1990
" Rev    : 1.00
" Chksm  : 6B20

"This pal divides the address space of the NS32CG160 into units
"of 64K word .
"It generates Chip Select to SRAM , ROM and Registers .

    ADEC        device 'P20R6';

"Control Inputs

CLK    pin 1;
OE     pin 13;

"Inputs

A17    pin 2;
A18    pin 3;
A19    pin 4;
A20    pin 5;
A21    pin 6;
A22    pin 7;
A23    pin 8;
A0     pin 9;
nHBE   pin 10;
nSHAD  pin 11;
nDDIN  pin 14;
nTSSO  pin 22;
nADSS  pin 23;

"Outputs

"async output
nCSSH  pin 15;

"sync output
nCSEP  pin 16;
nCSR0  pin 17;
nCSR1  pin 18;
```

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```

Tn0    pin 19;
Tn1    pin 20;
Tn2    pin 21;

x,c = .X.,.C.;
X = [.X.,.X.,.X.,.X.,.X.,.X.,.X.,.X.] ;
ADDR=[A23,A22,A21,A20,A19,A18,A17,x];
Tnum=[Tn2,Tn1,Tn0];

Equations

!nCSEP := nCSEP & ((ADDR==^h00) & !nSHAD # (ADDR==^h80)) & (!nADSS & nTSO)
        & !nDDIN # !nCSEP & !(Tnum==4) ;

" nCSEP = Chip Select EPROM for all the DATA BUS together (D0:D15)
" After RESET nSHAD=0 and the EPROM is mapped at address 0.

!nCSR0 := nCSR0 & (ADDR==^h00) & nSHAD & !A0 & (!nADSS & nTSO)
        # !nCSR0 & !(Tnum==1) ;

" nCSR0 = Chip Select SRAM , LOW DATA BUS (D0:D7)

!nCSR1 := nCSR1 & (ADDR==^h00) & nSHAD & !nHBE & (!nADSS & nTSO)
        # !nCSR1 & !(Tnum==1) ;

" nCSR1 = Chip Select SRAM , HIGH DATA BUS (D8:D15)

!nCSSH = (ADDR==^hf6) & !nTSO ;

" nCSSH = clock pulse to reset nSHAD bit (high) .

state_diagram Tnum

"This state machine is a sync machine , and used to find the last T3 .
"this machine is reset (state - 0) if nADSS=0 and nTSO=1
"and that is the R.E. of T2 .
"Every r.e. of cttl the state machine change state .
"The diffrent Chip Enable use this state machine .

state 0:
if (!nADSS & nTSO) then 0
else 1;

state 1:
if (!nADSS & nTSO) then 0
else 2;

```

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```

state 2:
if (!nADSS & nTSO) then 0
else 3;

state 3:
if (!nADSS & nTSO) then 0
else 4;

state 4:
if (!nADSS & nTSO) then 0
else 5;

state 5:
if (!nADSS & nTSO) then 0
else 6;

state 6:
if (!nADSS & nTSO) then 0
else 7;

state 7:
if (!nADSS & nTSO) then 0;

```

Test_vectors

```
([CLK,ADDR,nSHAD,A0,nHBE,nADSS,nTSO ]->[nCSEP,nCSR0,nCSR1,nCSSH,Tnum])
```

```
"test nCSEP in shedow address
```

```

[ c , X , 0 , x , x , 1 , 1 ]->[ 1 , 1 , 1 , 1 , x ]; "T1
[ c , ^h00 , 0 , x , x , 0 , 1 ]->[ 0 , 1 , 1 , 1 , 0 ]; "T2
[ c , ^h00 , 0 , x , x , 1 , 0 ]->[ 0 , 1 , 1 , 1 , 1 ]; "T3
[ c , ^h00 , 0 , x , x , 1 , 0 ]->[ 0 , 1 , 1 , 1 , 2 ]; "Tw
[ c , ^h00 , 0 , x , x , 1 , 0 ]->[ 0 , 1 , 1 , 1 , 3 ]; "Tw
[ c , ^h00 , 0 , x , x , 1 , 0 ]->[ 0 , 1 , 1 , 1 , 4 ]; "Tw
[ c , ^h00 , 0 , x , x , 1 , 0 ]->[ 1 , 1 , 1 , 1 , 5 ]; "T4

```

```
"test nCSSH
```

```

[ c , X , 0 , x , x , 1 , 1 ]->[ 1 , 1 , 1 , 1 , 6 ]; "T1
[ c , ^hf6 , 0 , x , x , 0 , 1 ]->[ 1 , 1 , 1 , 1 , 0 ]; "T2
[ c , ^hf6 , 0 , x , x , 1 , 0 ]->[ 1 , 1 , 1 , 0 , 1 ]; "T3
[ c , ^hf6 , 0 , x , x , 1 , 0 ]->[ 1 , 1 , 1 , 0 , 2 ]; "T4

```

```
"test nCSEP in it's real address
```

```

[ c , X , x , x , x , 1 , 1 ]->[ 1 , 1 , 1 , 1 , 3 ]; "T1
[ c , ^h80 , x , x , x , 0 , 1 ]->[ 0 , 1 , 1 , 1 , 0 ]; "T2
[ c , ^h80 , x , x , x , 1 , 0 ]->[ 0 , 1 , 1 , 1 , 1 ]; "T3
[ c , ^h80 , x , x , x , 1 , 0 ]->[ 0 , 1 , 1 , 1 , 2 ]; "Tw
[ c , ^h80 , x , x , x , 1 , 0 ]->[ 0 , 1 , 1 , 1 , 3 ]; "Tw
[ c , ^h80 , x , x , x , 1 , 0 ]->[ 0 , 1 , 1 , 1 , 4 ]; "Tw
[ c , ^h80 , x , x , x , 1 , 0 ]->[ 1 , 1 , 1 , 1 , 5 ]; "T4

```

```
"test nCSR0
```

```
[ c , X , 1 , x , x , 1 , 1 ]->[ 1 , 1 , 1 , 1 , 6 ]; "T1
```

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```

[ c , ^h00, 1 , 0, 1 , 0 , 1 ]->[ 1 , 0 , 1 , 1 , 0 ]; "T2
[ c , ^h00, 1 , 0, 1 , 1 , 0 ]->[ 1 , 0 , 1 , 1 , 1 ]; "T3
[ c , ^h00, 1 , 0, 1 , 1 , 0 ]->[ 1 , 1 , 1 , 1 , 2 ]; "T4
"test nCSR1
[ c , X , 1 , x, x , 1 , 1 ]->[ 1 , 1 , 1 , 1 , 3 ]; "T1
[ c , ^h00, 1 , 1, 0 , 0 , 1 ]->[ 1 , 1 , 0 , 1 , 0 ]; "T2
[ c , ^h00, 1 , 1, 0 , 1 , 0 ]->[ 1 , 1 , 0 , 1 , 1 ]; "T3
[ c , ^h00, 1 , 1, 0 , 1 , 0 ]->[ 1 , 1 , 1 , 1 , 2 ]; "T4

```

END

TL/EE/11090-4

```

module wait
flag '-r3' , '-t2' , '-s' , '-q2'

title 'APPLICATION NOTE : CPU:=NS32CG160 , MEMORY:=SRAM,EPROM '

" Author : Yiftach Shinar
" Date : 13 May 1990
" Rev : 1.00
"chksm : 0C26

```

```

"This pal generates the WAIT state by ~WAIT1 , ~WAIT2 .
"In this system the EPROM need 3 wait state ,
"and the SRAM need no wait state .

```

```

WAIT device 'P16R4';

```

"Control Inputs

```

CLK pin 1;
OE pin 11;

```

"Inputs

```

A17 pin 2;
A18 pin 3;
A19 pin 4;
A20 pin 5;
A21 pin 6;
A22 pin 7;
A23 pin 8;
nSHAD pin 13;
nDDIN pin 18;
nADSS pin 19;

```

"Outputs

```

nW1 pin 14;
nW2 pin 15;

```

```

x,c = .X.,.C.;
ADDR=[A23,A22,A21,A20,A19,A18,A17,x];
X = [.X.,.X.,.X.,.X.,.X.,.X.,.X.,.X.] ;

```

Equations

```

!nW1 := ((ADDR==^h00) & !nSHAD # (ADDR==^h80)) & !nADSS & !nDDIN;

```

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```
!nW2 := ((ADDR==^h00) & !nSHAD # (ADDR==^h80)) & !nADSS & !nDDIN;
```

```
Test_vectors
```

```
([CLK,ADDR,nSHAD,nADSS ]->[nW1 ,nW2  ])  
[ c , X , 0 , 1 ]->[ 1 , 1 ]; "T1  
[ c , ^h00, 0 , 0 ]->[ 0 , 0 ]; "T2  
[ c , ^h00, 0 , 1 ]->[ 1 , 1 ]; "T3  
[ c , ^h00, 0 , 1 ]->[ 1 , 1 ]; "Tw  
[ c , ^h00, 0 , 1 ]->[ 1 , 1 ]; "Tw  
[ c , ^h00, 0 , 1 ]->[ 1 , 1 ]; "Tw  
[ c , ^h00, 0 , 1 ]->[ 1 , 1 ]; "T4  
[ c , X , 0 , 1 ]->[ 1 , 1 ]; "T1  
[ c , ^hf6, 0 , 0 ]->[ 1 , 1 ]; "T2  
[ c , ^hf6, 0 , 1 ]->[ 1 , 1 ]; "T3  
[ c , ^hf6, 0 , 1 ]->[ 1 , 1 ]; "T4  
[ c , X , x , 1 ]->[ 1 , 1 ]; "T1  
[ c , ^h80, x , 0 ]->[ 0 , 0 ]; "T2  
[ c , ^h80, x , 1 ]->[ 1 , 1 ]; "T3  
[ c , ^h80, x , 1 ]->[ 1 , 1 ]; "Tw  
[ c , ^h80, x , 1 ]->[ 1 , 1 ]; "Tw  
[ c , ^h80, x , 1 ]->[ 1 , 1 ]; "Tw  
[ c , ^h80, x , 1 ]->[ 1 , 1 ]; "T4
```

```
END
```

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4.0 TIMING

The timing in this document is for NS32CG160-25.

4.1 SRAM—READ Cycle

Symbol	Description	Reference	Min	Max
t_{Av}	Address Valid	After R.E. T1	—	12
t_{Af}	Address Float	After R.E. T2	0	12
t_{ALEa}	ALE Active	After F.E. T4 or Ti	—	14
t_{ALEia}	ALE Inactive	After R.E. T1	—	14
t_{DDINv}	~ DDIN Valid	After R.E. T1	—	12
t_{TSOa}	~ TSO Active	After R.E. T2	—	12
t_{SOia}	~ TSO Inactive	After R.E. T4	—	12
t_{DBEa}	~ DBE Active	After F.E. T2	—	14
t_{DBEia}	~ DBE Inactive	After F.E. T4	—	12
t_{ACSRAM}	Chip Enable ACcess time SRAM	—	—	55
t_{HZSRAM}	Chip Disable to Output in High Z SRAM	—	—	25
t_{PD04}	74AS04 Propagation Delay D_N to Q_N	—	1	5
t_{PD373}	74AS373 Propagation Delay D_N to Q_N	—	—	6.5
t_{PD245}	74F245 Propagation Delay D_N to Q_N	—	2	7
t_{OE245}	74F245 Output Enable	—	2.5	9
t_{OD245}	74F245 Output Disable	—	2	7.5
t_{PDPAL}	Propagation Delay Input to Output PAL__10 ns	—	3	10
t_{COPAL}	Propagation Delay Clock to Output PAL__10 ns	—	2	8

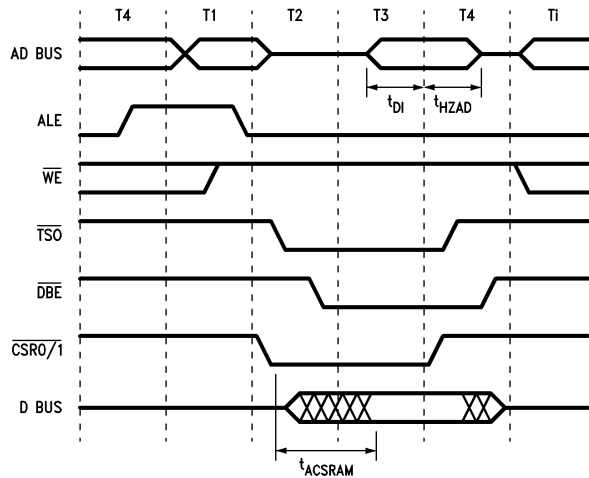
$t_{DI-SRAM}$ = Data-In set-up time—SRAM = $2T - t_{COPAL} - t_{ACSRAM} - T_{PD245} = 80-8-55-7$

$T_{DI-SRAM} = 10$ ns = data-in setup time for NS32CG160

$t_{HZAD} = AD$ BUS in High Z before R.E. $Ti/T1 = 0.5T - t_{DBEia} - t_{OD245} = 20-12-7.5$

$t_{HZAD} = 0.5$ ns

SRAM—READ CYCLE



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4.2 SRAM—WRITE Cycle

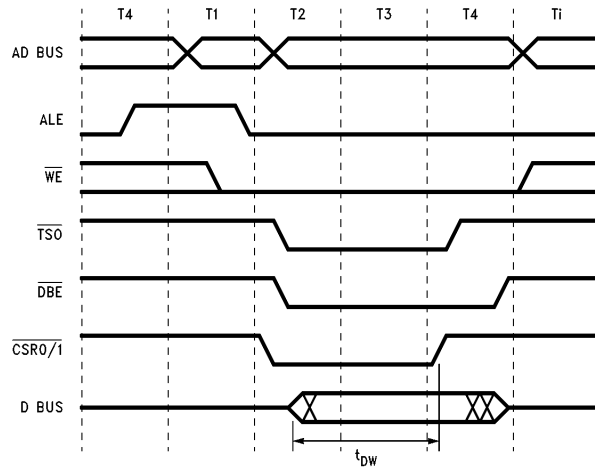
Symbol	Description	Reference	Min	Max
t_{Av}	Address Valid	After R.E. T1	—	12
t_{Dv}	Data-Out Valid	After R.E. T2	0	12
t_{ALEa}	ALE Active	After F.E. T4 or Ti	—	14
t_{ALEia}	ALE Inactive	After R.E. T1	—	14
t_{DDINv}	~ DDIN Valid	After R.E. T1	—	12
t_{TSOa}	~ TSO Active	After R.E. T2	—	12
t_{SOia}	~ TSO Inactive	After R.E. T4	—	12
t_{DBEa}	~ DBE Active	After R.E. T2	—	12
t_{DBEia}	~ DBE Inactive	After F.E. T4	—	12
t_{DWSRAM}	Data Valid to the End of Write SRAM	—	25	—
t_{PD04}	74AS04 Propagation Delay D_N to Q_N	—	1	5
t_{PD373}	74AS373 Propagation Delay D_N to Q_N	—	—	6.5
t_{PD245}	74AS245 Propagation Delay D_N to Q_N	—	2	7
t_{OE245}	74F245 Output Enable	—	2.5	9
t_{OD245}	74F245 Output Disable	—	2	7.5
t_{PDPAL}	Propagation Delay Input to Output PAL__10 ns	—	3	10
t_{COPAL}	Propagation Delay Clock to Output PAL__10 ns	—	2	8

$t_{DW} = \text{Data Valid to the End of Write} = 2T - t_{DBEa} - t_{OE245}$ or $2T - t_{Dv} - t_{PD245}$

$t_{DW-SRAM} = 80-12-9$ or $80-12-7$

$t_{DW-SRAM} = 59 \text{ ns}$ or $61 \text{ ns} > t_{DWSRAM}$

SRAM—WRITE CYCLE



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4.3 EPROM—READ Cycle

Symbol	Description	Reference	Min	Max
t_{Av}	Address Valid	After R.E. T1	—	12
t_{Af}	Address Float	After R.E. T2	0	12
t_{ALEa}	ALE Active	After F.E. T4 or Ti	—	14
t_{ALEia}	ALE Inactive	After R.E. T1	—	14
t_{DDINv}	\sim DDIN Valid	After R.E. T1	—	12
t_{TSOa}	\sim TSO Active	After R.E. T2	—	12
t_{SOia}	\sim TSO Inactive	After R.E. T4	—	12
t_{DBEa}	\sim DBE Active	After F.E. T2	—	14
t_{DBEia}	\sim DBE Inactive	After F.E. T4	—	12
t_{ACROM}	Address to Output Access time ROM	—	—	200
t_{HZROM}	Output Disable to Output in High Z ROM	—	—	55
t_{PD04}	74AS04 Propagation Delay D_N to Q_N	—	1	5
t_{PD373}	74AS373 Propagation Delay D_N to Q_N	—	—	6.5
t_{PD245}	74F245 Propagation Delay D_N to Q_N	—	2	7
t_{OE245}	74F245 Output Enable	—	2.5	9
t_{OD245}	74F245 Output Disable	—	2	7.5
t_{PDPAL}	Propagation Delay Input to Output PAL__10 ns	—	3	10
t_{COPAL}	Propagation Delay Clock to Output PAL__10 ns	—	2	8

$$t_{DI-EPROM} = \text{Data-In set-up-EPROM} = 6T-t_{Av}-t_{PD373}-t_{ACROM}-t_{PD245}$$

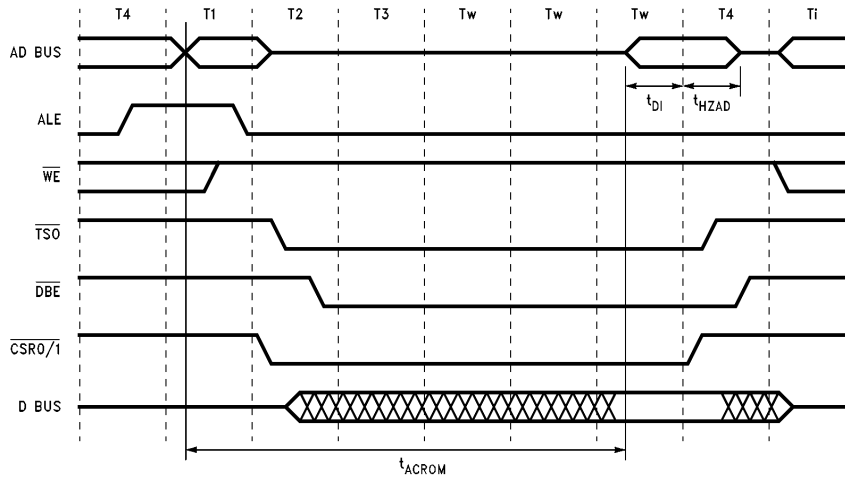
$$t_{dl-EPROM} = 240-12-6.5-200-7$$

$$t_{DI-EPROM} = 14.5 \text{ ns} > \text{data-in set-up time for NS32CG160}$$

$$t_{HZAD} = \text{AD BUS in High Z before R.E. Ti/T1} = 0.5-t_{DBEia}-t_{OD245} = 20-12-7.5$$

$$t_{HZAD} = 0.5 \text{ ns}$$

EPROM—READ CYCLE



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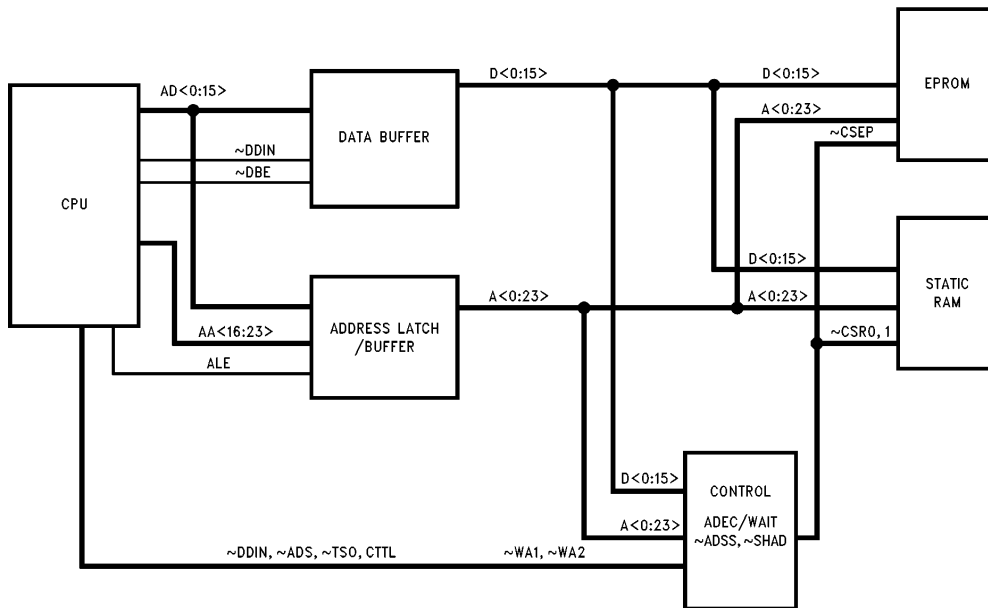
APPENDIX A

Bill of Materials

Number	Component	Qty.	Reference
(001)	IC NS32CG160-25	1	U1
(002)	IC P4C188-55	4	U9-U12
(003)	IC NMC27C512-20	2	U7-U8
(004)	IC 20R6-10	1	U6 Name: ADEC
(005)	IC 16R4-10	1	U22 Name: WAIT
(006)	IC 74AS04	1	U14
(007)	IC 74AS74	1	U21
(008)	IC 74AS244	2	U15, U23
(009)	IC 74AS373	2	U4-U5
(010)	IC 74F245	2	U2-U3
(011)	Crystal Oscillator—50 MHz	1	U13
(012)	RES - SIP8PULL—10k	2	RP1-RP2
(013)	RES - Discrete—4.7k	1	R1
(014)	CAP/C 0.1 μF	1	C1
(015)	DIODE 1N914	1	D1
(016)	Push-Bottom	1	SW1

APPENDIX B

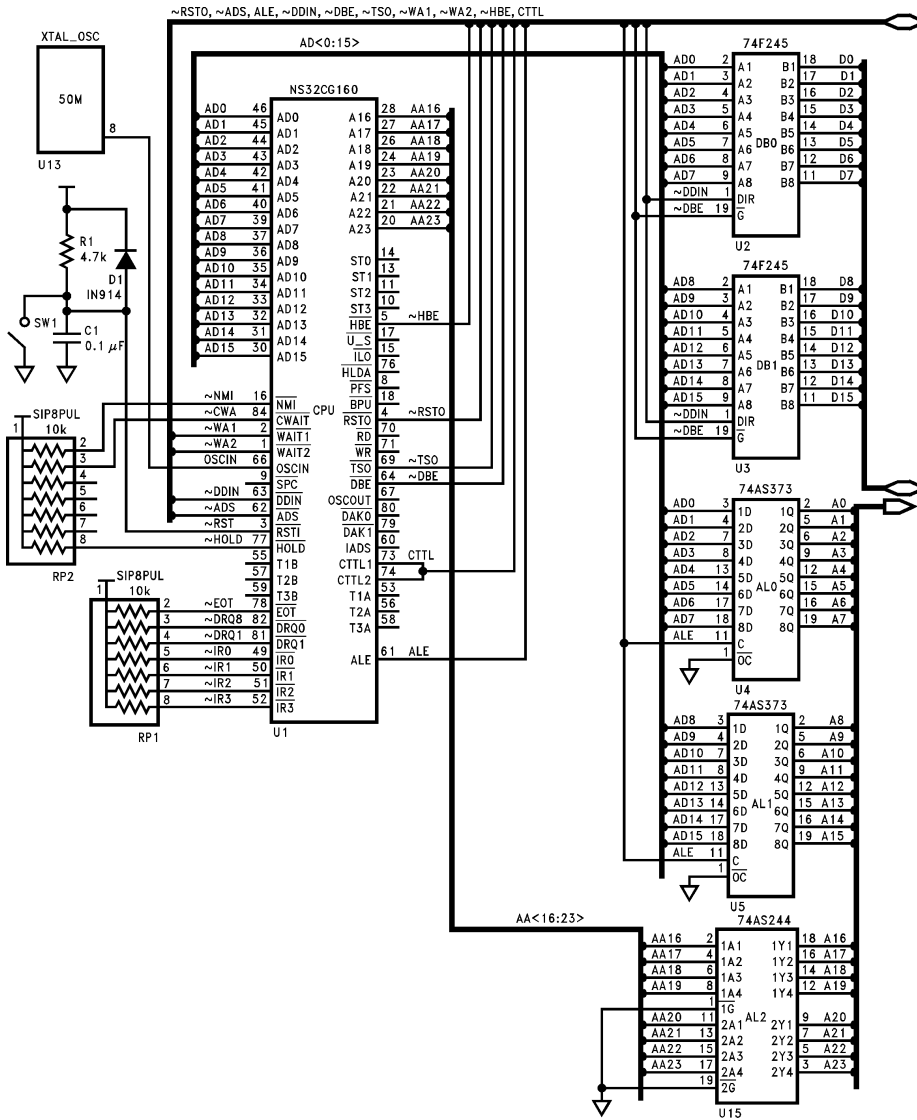
Block Diagram



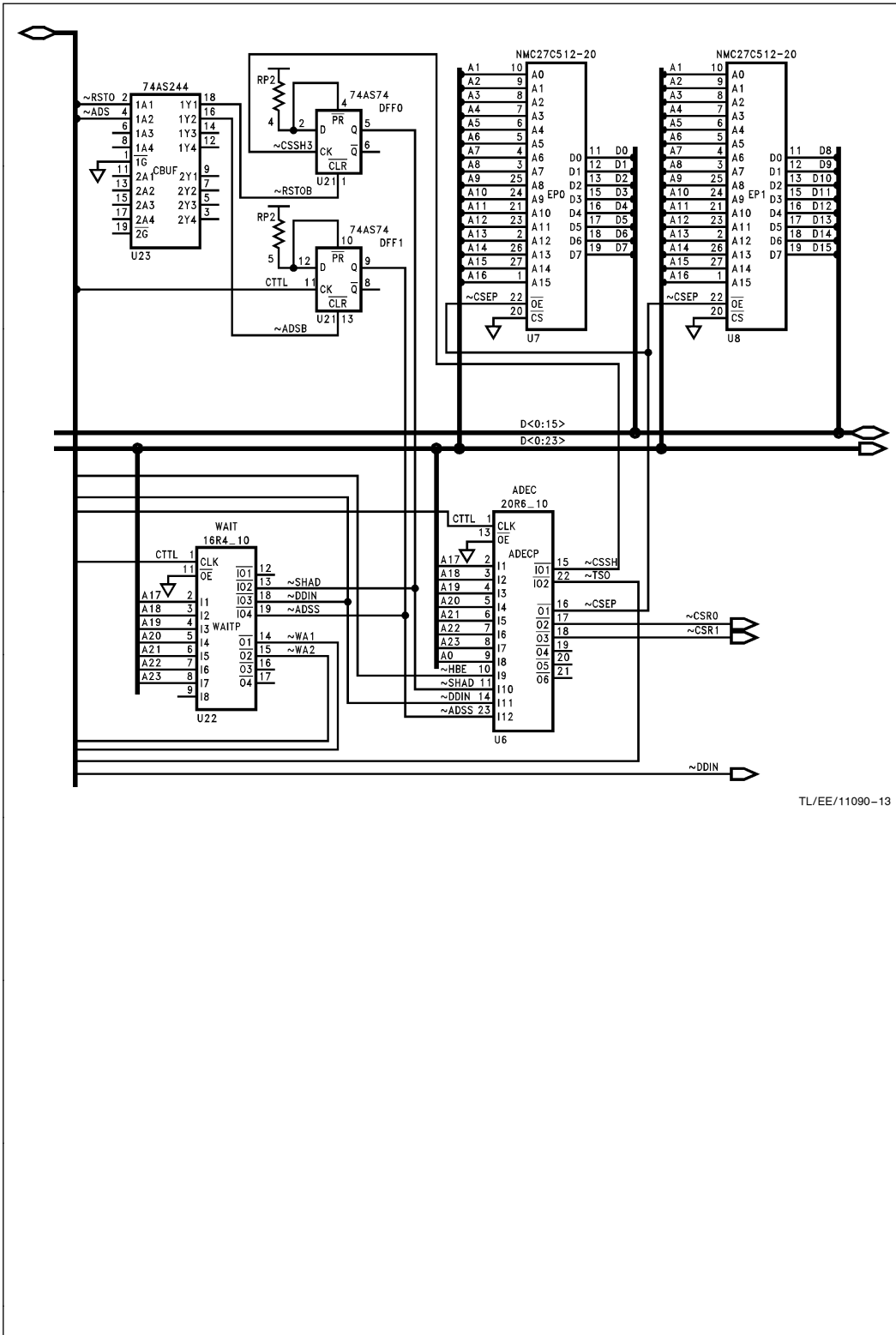
TL/EE/11090-10

APPENDIX C

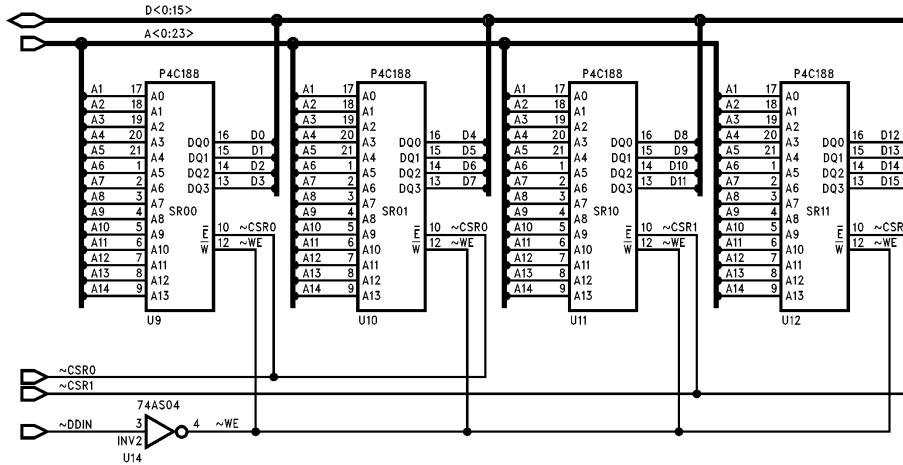
Electrical Schematics



TL/EE/11090-11



TL/EE/11090-13



TL/EE/11090-12

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